COURSE DESCRIPTION CARD - SYLLABUS

Course name
Internet Przedmiotów/Internet of Things

Course

Field of study
Computing

Year/Semester
2/3

Area of study (specialization)
Artificial Intelligence

Profile of study
general academic

Level of study
Second-cycle studies

Course offered in
Polish

Form of study
full-time

Requirements
compulsory

Number of hours

Lecture	Laboratory classes	Other (e.g. online)
30	30	
Tutorials	Projects/seminars	

Number of credit points

5

Lecturers

Responsible for the course/lecturer:
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Faculty of Computing and Telecommunication
Institute of Computing Science

Responsible for the course/lecturer:

Prerequisites

A student starting this course should have a basic knowledge of digital and analog electronics. He should have knowledge to be able to solve a basic problems in the area of testing/measurements simple digital and anolog circuits. He should also have the ability to obtain information from the indicated sources and be ready to cooperate as part of a team. In the area of social competence, he must present attitudes such as honesty, responsibility, perseverance, cognitive curiosity, creativity, personal culture, and respect for other people.

Course objective

To acquaint the student with the techniques of digital modeling and simulation (VHDL).
Provide students with basic knowledge of analog circuit modeling using SPICE.
Provide students with basic knowledge in the field of mixed analogue-digital models using the VHDL-AMS language.
To acquaint students with the methods of behavioral and structural description of mixed systems in the

VHDL / VHDL-AMS language.
To familiarize the student with the methods of describing test systems (testbench) in VHDL language.
Shaping teamwork skills in students by modeling a digital system with the use of components prepared by individual group members..

Course-related learning outcomes

Knowledge

The student has advanced and in-depth knowledge of broadly understood information systems, theoretical foundations of their construction and the methods, tools and programming environments used for their implementation (K2st_W1)
The student has advanced detailed knowledge of selected issues in the field of computer science (K2st_W3).
The student knows the development trends and the most important new achievements of computer science and other selected related scientific disciplines (K2st_W4).
The student has advanced and detailed knowledge of the processes taking place in the life cycle of hardware or software information systems (K2st_W5).
The student knows advanced methods, techniques and tools used in solving complex engineering tasks and conducting research in a selected area of computer science (K2st_W6)

Skills

The student is able to obtain information from literature, databases and other sources (in Polish and English), integrate them, make their interpretation and critical evaluation, draw conclusions and formulate and exhaustively justify opinions (K2st_U1).
The student is able to use analytical, simulation and experimental methods to formulate and solve engineering tasks and simple research problems (K2st_U4).
The student is able - when formulating and solving engineering tasks - to integrate knowledge from various areas of computer science (and, if necessary, also knowledge from other scientific disciplines) and apply a system approach, also taking into account non-technical aspects (K2st_U5).
The student is able to assess the usefulness and the possibility of using new achievements (methods and tools) and new IT products (K2st_U6).
The student is able to interact in a team, assuming different roles in it (K2st_U15)

Social competences

The student understands that in computer science, knowledge and skills very quickly become obsolete (K2st_K1).
He understands the importance of using the latest knowledge in the field of computer science in solving research and proctical problems (K2st_K2).

Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:

The exam consists of the theoretical and problematic parts. In the theoretical part, the student answers basic questions in the field of modeling and simulation methods for analog circuits using the SPICE language and digital ones using the VHDL language. Knowledge, presented druing the lectures, related

to the exmaple circuits (A/D & D/A conversters) will be also required. In the problem part, the student develops a model of a given digital circuit described in VHDL and a model of the testbench system. 51% of both parts of the exam are required.

The assessment from the laboratory part is the result of the following assessments:
- assessment of the student's preparation for laboratory classes (prepared model of a given circut) and assessment of skills related to the model implementation and simulation during the laboratory classes.
- evaluation for the presentation/defense of the task performed as part of individual laboratory exercises.
- evaluation of the report prepared partly during the classes and partly after its completion; this assessment also includes teamwork.

Programme content

Lecture topics:

VHDL hardware description language - language syntax, design unit structure, behavioral, structural and mixed description of digital circuits in VHDL;
Methods of describing test systems (testbench) in VHDL language;
Operation and capabilities of the VHDL language simulator (based on the MODELSIM program by Mentor Graphic;
Methods for describing analog circuits using the SPICE language/simulator - syntax, types of analyzes;
VHDL-AMS language for modeling and simulating mixed circuits.
In order to illustrate the above modeling and summation methods, selected structures of analog-to-digital converters (sigma-delta, double integration) and methods of determining their parameters will be presented.

Laboratory topics:

Students will learn modeling and simulation methods on the example of computer tools included in the Mentor Graphics system:
- Getting to know the operation of the MODELSIM simulation program;
- Preparation of a simple test environment - generation of forces in VHDL;
- Behavioral description of basic digital blocks in VHDL;
- Synthesizable description of digital blocks;
- Testbench with the use of complex VHDL structures - tables, records, files;
- Design of a complex digital circuit using libraries, packages, generic and other capabilities of the VHDL language. Behavioral model, synthesizable, testbench, development of project documentation using the capabilities of Mentor Graphics.
- Characterization of A / D converters using SCILAB / MATLAB software

Teaching methods

Lectures: multimedia presentations, illustrated with examples given on the blackboard.

Laboratory exercises: practical exercises with the use of SPICE and MODELSIM simulation programs (VHDL simulator), discussion, team work, case studies.
Design and implementation of digital circuit models, and then building a larger digital system model using prepared components.

Bibliography

Basic

1. M. Zwoliński, Projektowanie układów cyfrowych wykorzystaniem języka VHDL, WKŁ 2007.

2. K.Skahill, Język VHDL-Projektowanie programowalnych układów logicznych, WNT, 2004.

3. P.J.Ashenden, G.D.Peterson and D.A. Teegarden, The System Designer's Guide to VHDL-AMS”, Morgan Kaufmann Publishers, 2002.

Additional

1. Charles H. Roth, Jr., Digital Systems design Using VHDL, PWS Publishing Company, 1998.

2. P. Śniatala, M. Kropidłowski, S. Szczęsny, J. Goes, N. Paulino and J. Pedro Oliveira, "Current Mode Sigma-Delta Modulators Designed for Amperometry Based Medical Sensors," 2018 International Conference on Signals and Electronic Systems (ICSES), Kraków, Poland, 2018, pp. 47-52.

3. S. Yalamanchili, Introductory VHDL From Simulation to Synthesis, Prentice Hall, 2000.

4. J.Bhasker, VHDL Primer, Prentice Hall, 1999.

Breakdown of average student's workload

	Hours	ECTS
Total workload	120	5,0
Classes requiring direct contact with the teacher	65	3,0
Student's own work (literature studies, preparation for laboratory classes/tutorials, preparation for tests/exam, project preparation) [1]	55	2,0

[1] delete or add other activities as appropriate